

Overview

In this unit your students should:

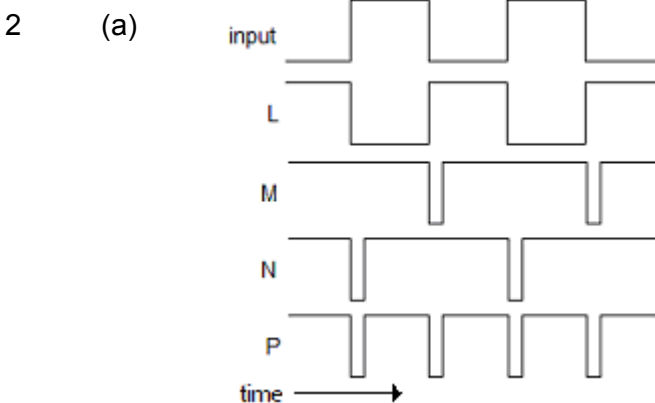
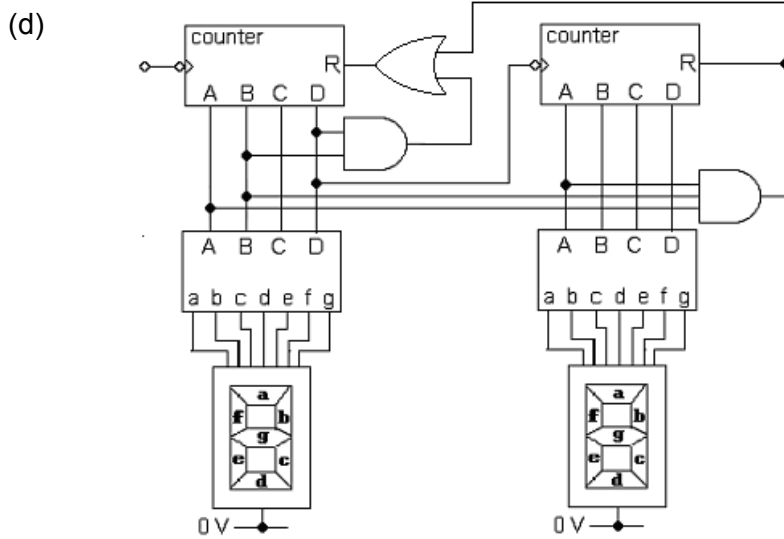
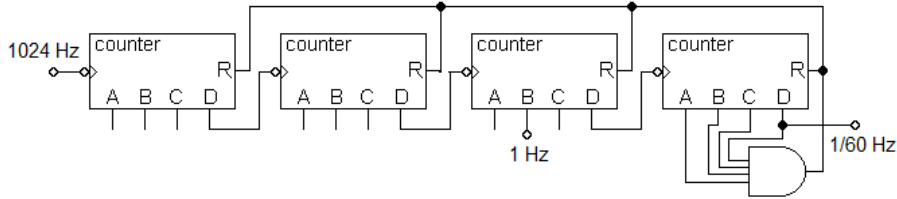
- meet the use of a crystal oscillator
- find out how binary counters can be used for frequency division
- understand why crystal oscillators are used instead of relaxation oscillators in clocks
- investigate the use of frequency doublers in frequency division

This should not require more than 3 hours of class time.

Hour	Suggested Activity
1	<p>Launch students straight into the Timing circuits practical. This will introduce them to crystal oscillators and let them investigate the use of binary counters for frequency division. Steps 4 and 5 are extension activities.</p> <p>Ask them to answer questions 1 and 2 of the Clocks exercises.</p>
2	<p>Discuss their answers to the first page of the Clocks exercises.</p> <p>Get them to answer questions 3, 4 and 5 of the Clocks exercises.</p> <p>As they finish, get them started on the Frequency division practical. They will have some of the components already on their breadboard. They will have a chance to finish off the practical next session.</p> <p>Ask them to answer questions 1 and 2 on page 117 of the text book before the next session.</p>
3	<p>Students who have successfully answered both questions from the text book should continue with the Frequency division practical. Step 5 will keep them busy.</p> <p>Spend time with students who need help with the text book questions, before allowing them to continue with the practical.</p> <p>Ask them to study 7.3 from the text book and answer questions 1 and 2 of the Continuous Sequencers exercises before the next session.</p>

Model Answers

- 1 (a) A crystal oscillator has a known stable frequency which is a convenient power of 2. Relaxation oscillators use components whose values have a tolerance of perhaps $\pm 5\%$, so their frequency can vary by quite a bit from one oscillator to the next.
- (b) $1024 = 2^{10}$, so ten one-bit counters will be required.
- (c) One minute requires 60 one-second pulses. The binary for 60 is 111100, so the AND gate resets the whole counter chain once a minute.



- (b) Five cycles of the signal at the input creates ten pulses at P. These are counted by the counter, which is reset every five pulses by the AND gate connected to C and A (CBA = 101 is five). So five cycles at the input result in two clock pulses for the one-bit counter, causing one cycle of signal at the output.