Overview

In this unit your students should:

- learn about the behaviour of a D flip-flop
- understand the significance of edge-triggering
- find out how a D flip-flop can be made from a master-slave arrangement of latches
- understand how a register is made from flip-flops
- appreciate the role of registers in processing binary words

This should not require more than 3 hours of class time.

Hour	Suggested Activity
1	Launch them straight into the **D flip-flops** practical. The first three parts should help them to discover the behaviour of a D flip-flop, and the last part will allow them to apply what they have learnt. Ask them to study **5.3** before the next session.
2	Get them to work through the **Flip-flops** exercises, using the text book if necessary. Discuss their answers to the exercises. Use a short informal test to find out what they have learnt about the effect of the various inputs to a D flip-flop.
3	Students should work through questions 1, 2 and 3 on pages 80 and 81 of the text book. Keep an eye on their answers, and insist on accurate timing diagrams and complete written explanations. Ask them to revise **Storing Signals** for a formal test next session.

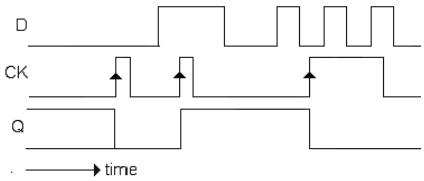
Model Answers

1 (a) Pulsing S high sets the flip-flop, with Q = 1 and $\overline{Q}$ = 0.

Pulsing R high resets the flip-flop, with Q = 0 and $\overline{Q}$ = 1.

(b) Data is only transferred from D to Q as the clock terminal is rising from 0 to 1. At all other times, Q is frozen.

(c)



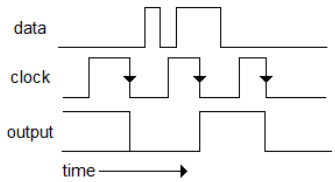
2 (a) A latch is transparent when the signal at D is copied to Q. When the latch is frozen, the signal at Q remains constant, regardless of any changes to the signal at D.

(b)

clock	left-hand	right-hand
0	F	T
1	T	F

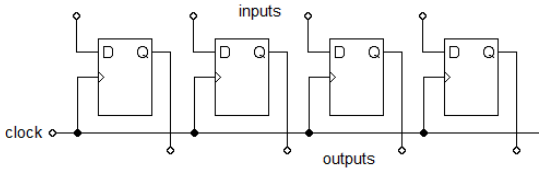
(c) When **clock** is 1, signals at **data** are present at the D input of the right-hand latch. Lowering **clock** to 0 makes that latch transparent, allowing the instantaneous signal at **data** through to the output. At the same time, the left-hand latch is frozen, so subsequent changes at **data** do not reach the D input of the right-hand latch. Raising **clock** back up to 1 has no effect on **output** because the right-hand latch freezes before signals at **data** have time to get through the left-hand latch as it becomes transparent.

(d)



3 (a) The four-bit word at the inputs is copied to the outputs upon each rising edge at CK. In between rising edges at CK, the word at the outputs is frozen.

(b)



(c) (i) Raising CK high copies 0110 into register A and 1101 into register B, but has no effect on the final output register. The AND gates present 0100 at the input of the final register (only generating a 1 when both inputs are 1).

(ii) Putting CK low copies 0100 to the outputs of the final register, but has no effect on the A or B registers.