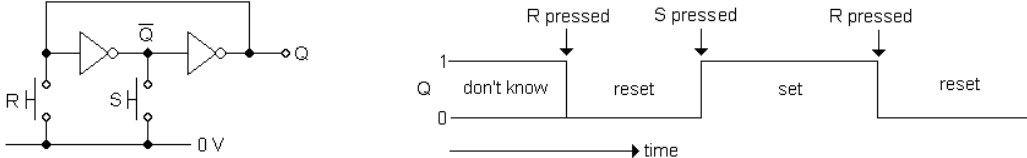


Overview

In this unit your students should:

- learn the meaning of the terms set and reset
- meet the use of NAND and NOR gates to make bistables
- know how to represent the behaviour of bistables with timing diagrams
- learn that NOR gate bistables have active-high inputs
- understand why NAND gate bistables have active-low inputs

This should not require more than 2 hours of class time.

Hour	Suggested Activity
1	<p>Introduce students to this NOT gate bistable and summarise its behaviour with a timing diagram. Make sure that they understand the meaning of set and reset.</p>  <p>Launch students into the Exploring bistables practical. Ask students to study 5.1 of the text book before the next session.</p>
2	<p>Get students to work through the Bistables exercises. As they finish, get them to start answering questions 1 and 2 on page 79 of the text book. As well as finishing off the questions before the next session, ask students to study 5.2 of the text book.</p>

Model Answers

1 (a) A bistable is **set** when its output is high. It is **reset** when its output is low.

(b)

S	Q	P
0	0	1
0	1	0
1	0	0
1	1	0

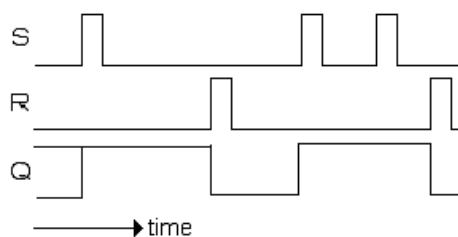
(c) The truth table shows that when S = 0, P can be 1 or 0, with Q = 0 or 1.

The equivalent table for the other gate would show that Q can be 1 or 0 when R = 0.

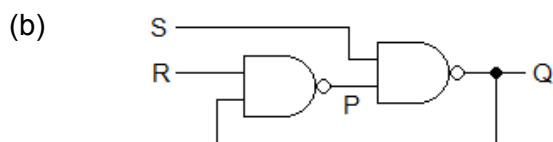
(d)

S	R	Q
0	0	1 or 0
1	0	1
0	1	0

(e)



2 (a) An active-low input must be brought low for it to have the required effect on the system.



(c) $Q = \bar{S} + \bar{P} = \bar{S} + \overline{Q.R} = \bar{S} + Q.R$

So when S = 0, Q has to be 1 regardless of the state of Q or R.