

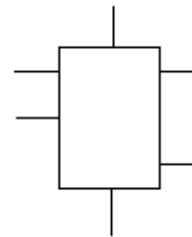
1 Link each **term** used for a D flip-flop with its **meaning**.

term
set
clock
reset
rising edge
falling edge
complementary

meaning
outputs with different states
signal going from low to high
signal going from high to low
input which forces output low
input which forces output high
input which accepts triggering edges

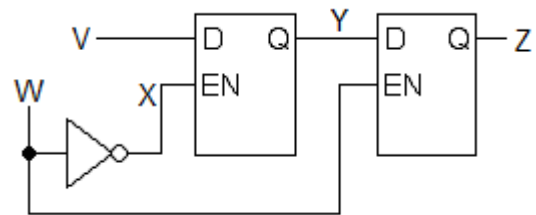
2 Label the inputs and output of this flip-flop.  
Use these words.

**clock**      **data**                      **inverted output**  
**non-inverted output**              **reset**                      **set**



3 Complete the sentences for this master-slave flip-flop. Choose from these symbols.

**V**      **W**      **X**      **Y**      **Z**



While W is low, the bit to be stored is placed at \_\_\_\_\_. The bit appears at \_\_\_\_\_ because \_\_\_\_\_ is high, making the latch transparent. However, the bit at \_\_\_\_\_ is frozen as \_\_\_\_\_ is low. Pulling \_\_\_\_\_ high allows the bit at \_\_\_\_\_ to be copied to Z.  
While W is high, the bit at \_\_\_\_\_ is frozen, therefore any changes at \_\_\_\_\_ don't affect the state of \_\_\_\_\_. Pushing W low freezes the state of \_\_\_\_\_ once more.

4 Label each row of this timing diagram for a D flip-flop.  
Choose from these words.

**set**  
**data**  
**reset**  
**clock**  
**output**

