

Overview

In this unit your students should:

- meet Boolean expressions for NAND, NOR and EOR gates
- be able to use De Morgan's, Race Hazard and Redundancy Theorems
- know how to make basic logic gates out of just NAND gates

This should not require more than 2 hour of class time.

Hour	Suggested Activity
1	<p>Remind students of the three theorems they encountered in their preparation for this session: De Morgan's, Race Hazard and Redundancy.</p> <p>Get students to work through the Logic System Design exercises. Encourage them to work out each expression of question 3 step by step, using the theorems, rather than just guessing.</p> <p>Ask them to study 4.3 before the next session.</p>
2	<p>Launch students straight into the All from NAND gates practical.</p> <p>Work through an example of designing a logic system from just NAND gates. Include the use of De Morgan's Theorem to represent NAND gate behaviour with $\overline{X.Y} = \overline{X} + \overline{Y}$.</p> <p>Ask them to answer the questions on page 1 of the Only NAND gates exercises before the next session.</p>