

Overview

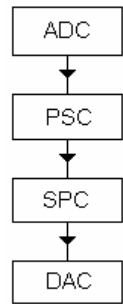
In this unit your students should:

- be able to design flash and slope ADCs
- be able to assemble SIPO and PISO registers from flip-flops
- understand the advantages and limitations of sending analogue signals in digital format

This should not require more than 5 hours of class time.

Hour	Suggested Activity
1	<p>Launch your students straight into the Flash converter practical. They will need help from the textbook to design the logic system required in step 5. Step 7 is extension work.</p> <p>Ask them to study 8.1 before the next session.</p>
2	<p>Students could use this session to work through the first page of the Digital transmission exercises.</p> <p>As they finish, they could start the Slope conversion practical. They will be able to finish it during the next session.</p> <p>Ask them to answer questions 1 and 2 on page 158 of the textbook before the next session.</p>
3	<p>Allow students to complete the Slope conversion practical. Step 8 is extension work.</p> <p>As they finish, get them to work through the second page of the Digital transmission exercises.</p> <p>Ask them to answer questions 3 and 4 on page 158 of the textbook before the next session.</p>
4	<p>Students should use this session to do the Serial output ADC practical.</p> <p>As they finish, get them to work through question 9 of the Digital transmission exercises.</p> <p>Ask them to answer questions 10 to 13 of the Digital transmission exercises before the next session.</p>
5	<p>Discuss their answers to questions 10 to 13 of the Digital transmission exercises.</p> <p>Students should then answer question 5 on page 159 of the textbook.</p> <p>As they finish, they could do the Sampling distortion practical, unless they need to spend more time on the questions from the textbook.</p> <p>Ask them to study 8.2 before the next session</p>

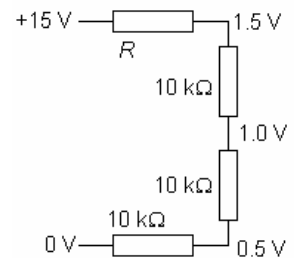
Model Answers



- 1 (a)
- (b) The ADC samples the incoming analogue signal at regular intervals, coding the voltage of each sample as a binary word. The PSC transmits this word one bit at a time along the transmission link. The SPC at the other end of the link takes the bits as they arrive and assembles them back into binary word which can be passed on to the DAC for conversion back into a voltage.
- (c) Digital signals can have noise and interference removed at the receiver. They can also be compressed, speeding up data transmission rates. Neither of these techniques can be applied to analogue signals.
- (d) The process of analogue-to-digital conversion only retains some of the information in the original signal. The reconstituted signal in the receiver can only have one of a limited number of voltages and signals above half the sampling frequency will not be present.

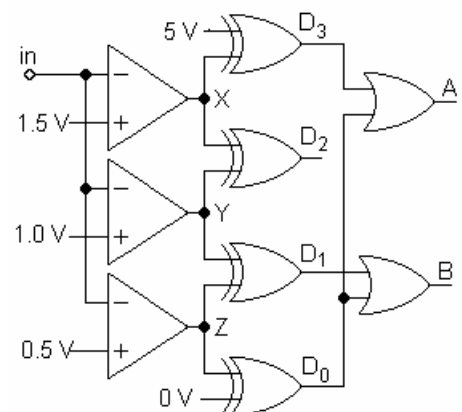
- 2 (a) The conversion time is how long it takes for the ADC to produce a binary word from a sampled voltage. The word can only code for voltages between 0 V and 1 V, with adjacent words coding for voltages which are 2 mV apart.
- (b) number of levels = $\frac{1.00}{2 \times 10^{-3}} = 500$. A nine bit word produces $2^9 = 512$ different combinations, enough for 500 different levels.
- (c) $f = \frac{1}{T} = \frac{1}{125 \times 10^{-6}} = 8 \times 10^3$ Hz, so since you need to sample at least twice in each cycle, the analogue signals should be kept below 4×10^3 Hz or 4 kHz.

- 3 (a) The bottom three resistors have the same voltage drop, so need the same value (e.g. 10 kΩ).
 For each 10 kΩ: $I = \frac{V}{R} = \frac{0.5}{10 \times 10^3} = 50 \times 10^{-6}$ A
 For R: $R = \frac{V}{I} = \frac{15 - 1.5}{50 \times 10^{-6}} = 270 \times 10^3 \Omega$ or 270 kΩ

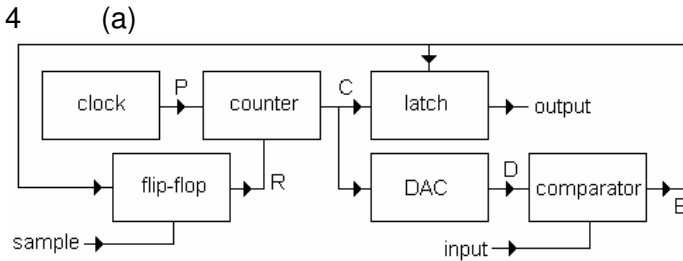


(b)

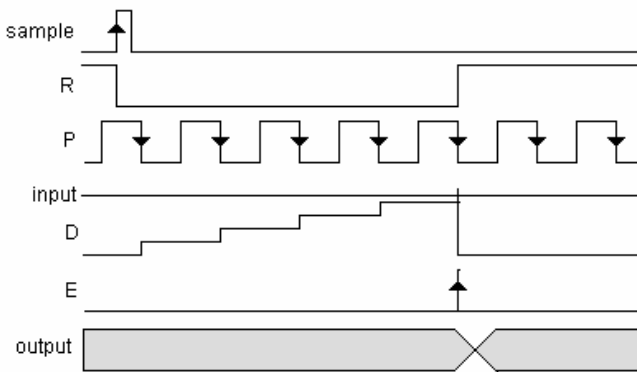
in	X	Y	Z	D ₃	D ₂	D ₁	D ₀	B	A
0.0 V	1	1	1	0	0	0	1	1	1
0.5 V	1	1	0	0	0	1	0	1	0
1.0 V	1	0	0	0	1	0	0	0	0
1.5 V	0	0	0	1	0	0	0	0	1



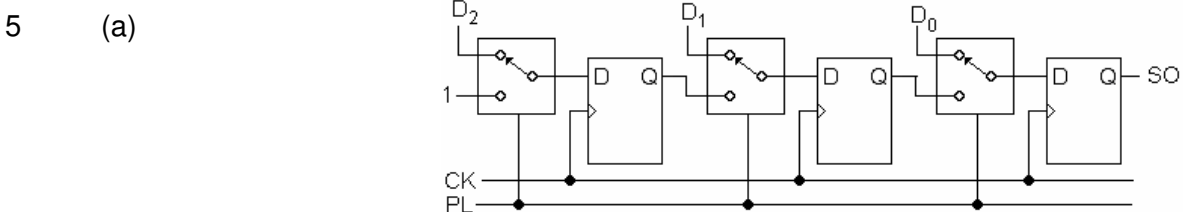
- (c) The op-amps compare the signal at **in** with the three reference signals to produce signals at X, Y and Z shown in the table. (The op-amp outputs have been processed to convert saturation levels of ± 13 V in to +5 V and 0 V.) The EOR gates compare adjacent op-amp output signals, giving a 1 only if they are different. Those signals are then combined with OR gates to produce the output word, as shown.



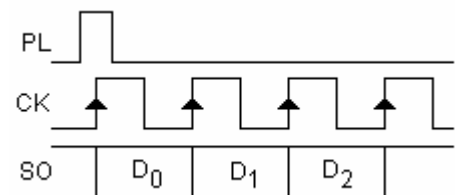
- (b) The system is triggered by a rising edge at **sample**. This sets the flip-flop so that R goes low and the counter can respond to pulses at P. As the count at C increases, the output D of the DAC goes up in steps until it goes above the signal at **input**. This is detected by the comparator whose output E goes high, triggering the latch into copying C to **output** and resetting the flip-flop and forcing the counter back to zero until the next rising edge at **sample**.



- (c) $2^6 = 64$, so the counter requires a six-bit word.
 Each clock pulse moves the DAC output up one level, so clock speed must be $6\,800 \times 64 = 435\,200 \text{ s}^{-1}$ or 435 kHz.
- (d) A flash converter has a much faster conversion time than a slope conversion one.



- (b) The first rising edge at CK has PL high, so each flip-flop is loaded with one bit of the input word $D_2D_1D_0$. The next three rising edges at CK have PL low, so they copy the output of each flip-flop to the next one along.



So D_0 , D_1 , D_2 and 1 appear at
SO one after the other.

