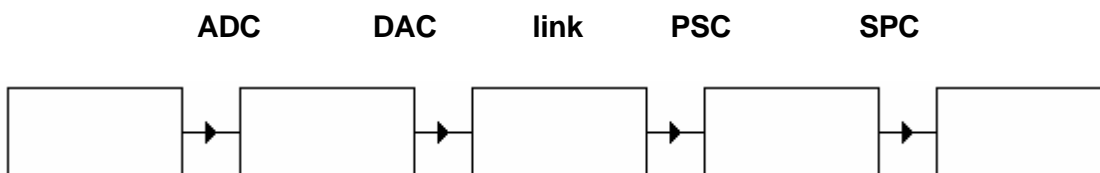


1 Complete the block diagram for a digital transmission system. Use these blocks.

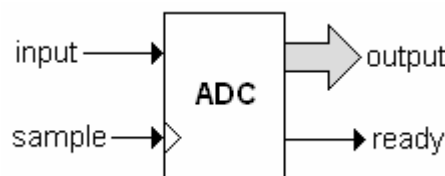


2 Link each **block** of a digital transmission system with its **function**.

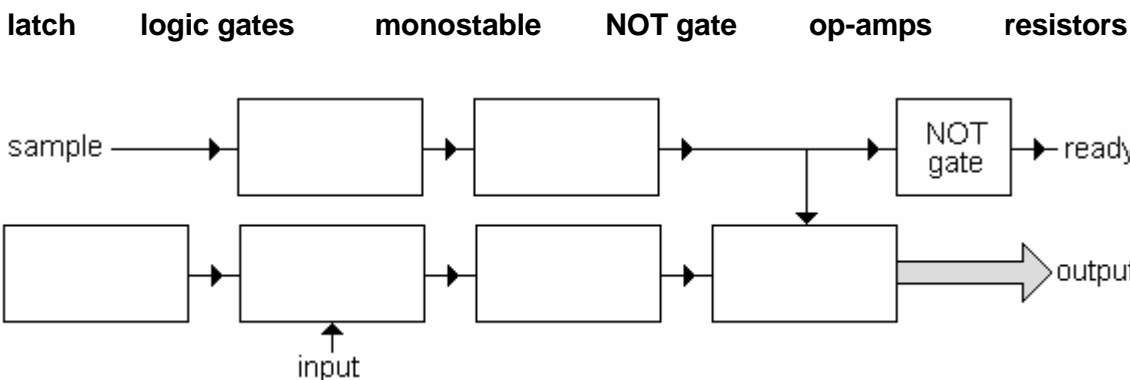
block	function
ADC	outputs a word one bit at a time
PSC	voltage at output depends on word at inputs
link	outputs words which code for the input voltage
SPC	transfers information as a steady stream of bits
DAC	latches bits one after the other to create a word

3 Complete the sentences for the ADC.

Initially, _____ is high. It goes low each time a rising edge arrives at _____. It goes high again once the word at _____ represents the voltage at _____.



4 Complete the block diagram for a flash converter. Use these blocks.



5 Here are some statements about digital transmission systems. Which of them are true?

- Any analogue signal can be transmitted.
- Doubling the sample rate always halves the word length.
- All the information in the analogue signal can be transmitted.
- Increasing the word length improves the quality of the transmission.
- The digital stream can be compressed to speed up transmission rates.
- The signal can usually be completely restored when it emerges from the link.

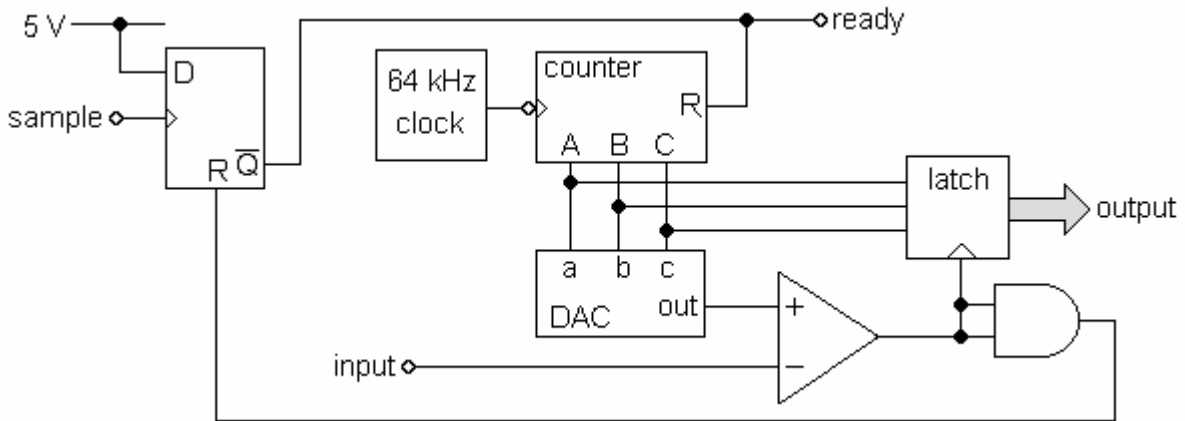
6 Link each **term** for an ADC with its **meaning**.

term	meaning
range	number of lines in the output bus
resolution	how many times the system codes the input voltage in one second
word length	smallest change of input voltage which results in a change of word at the output
sample rate	the time it takes for the output word to stabilise after the system has been triggered
conversion time	difference between maximum and minimum voltage at input which can be coded

7 Complete the table for flash converters.

resistors	op-amps	word length	range	resolution
4	3	2 bits	2.0 V	0.5 V
8			4.0 V	
		5 bits		0.1 V
	255		5.12 V	

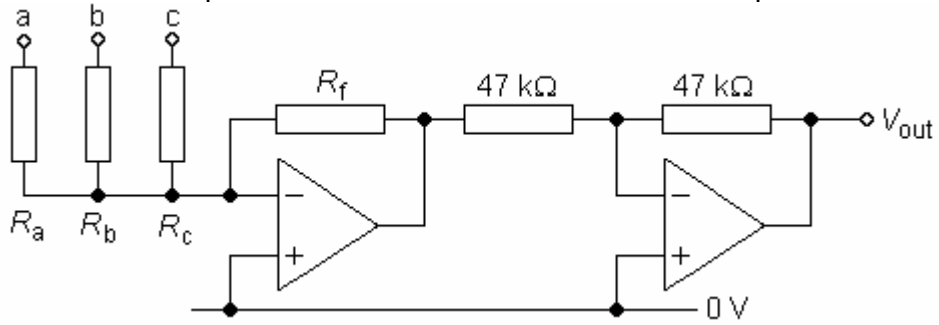
8 Complete the sentences for this slope converter.



The system is triggered by feeding a _____ into _____.
 This makes _____ go low, allowing the _____ to count pulses from the _____. The output of the _____ feeds into the _____. The voltage at _____ goes up in steps. As soon _____ is at a higher _____ than _____, the _____ is triggered. Shortly afterwards the _____ is reset and _____ returns _____.

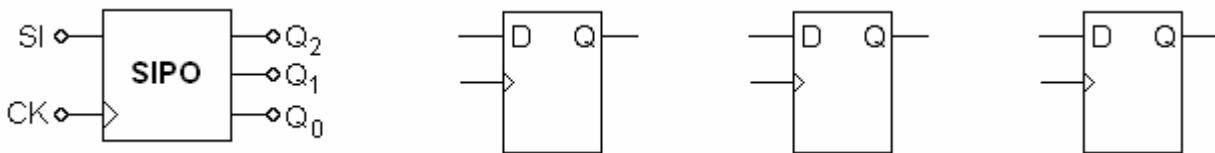
The output is a ___-bit word. The maximum _____ is 125 μ s, limiting the maximum sample rate to _____ kHz. The sample rate can be increased by _____ the word length or _____ the clock speed.

9 Do calculations to complete the table for this DAC. Assume the inputs are at +5 V or 0 V.

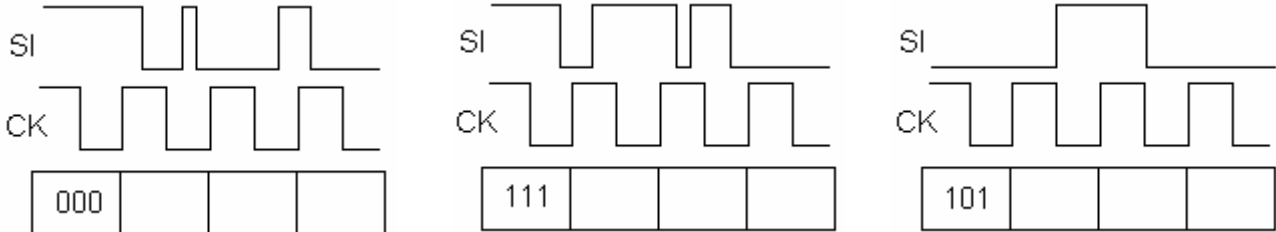


R_a	R_b	R_c	R_f	range	resolution
120 kΩ	60 kΩ		24 kΩ		1.0 V
	160 kΩ			1.4 V	
			10 kΩ		0.25 V

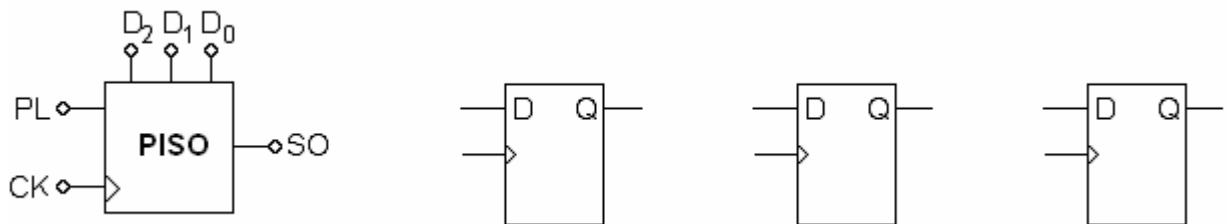
10 Complete the circuit on the right to make the three-bit SIPO shift register on the left. Label all the terminals.



11 The timing diagrams are for the SIPO shift register above. Complete the words in the boxes.



12 Complete the circuit on the right to make the three-bit PISO shift register on the left.



13 Complete this timing diagram for the PISO shift register above. The word at the input when PL goes high is 011.

